**Digital Design 2 Fall 2020**

**Dr Mohamed Shaalan**

**Project 2: Automated Clock Gating**

**First Prototype**

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**Plan:**

1. Read the Verilog netlist file and parse it using pyverilog.
2. After parsing, we fix the netlist to use the clock gating.
3. This should lead to decrease the power consumption
4. Then we generate the enhanced Verilog code in the netfile.

**Language:**

We will use python in order to use PyVerilog to make it a lot easier to parse and modify the netlist since languages such as C++ will require us to parse the netlist ourselves.

**Libraries:**

We are going to use PyVerilog a tool-kit for RTL design analysis. It consists of code parser, dataflow analyzer ,control-flow analyzer and code generator.